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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,919	HWANG ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 10/27/2003. Claims 1-20 are pending.

Claim Objections

Claims 3, 10, and 12 are objected to because of the following informalities: the word " attempting" in these claims is not a definite claim language. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-3, 8-14, 16, and 20** are rejected under 35 U.S.C. 102(b) as being unpatentable by **Wallace** (US Patent No. 6360352).

Referring to claim l, Wallace discloses the method for mapping a user function for a programmable integrated circuit to a plurality of lookup tables, the method comprising:

decomposing the user function into a first set of decomposed functions (*Wallace teaches the step of decomposition a design circuit ("user function") into one or more fanout-free regions ("decomposed functions"); col. 1, lines 40-45, lines 61- 65; col. 2, lines 1-6; col. 4, lines 53+; col. 5, lines 1-28; col. 8, lines 13-19; col. 14, lines 45-56)*, the user function receiving input variables (*Fig. 1; col. 2, lines 15-16*);

determining whether the first set of decomposed functions can be implemented

by one of a set of lookup table configurations for the programmable integrated circuit; and

if none of the set of lookup table configurations can implement the first set of decomposed functions, rotating at least two of the input variables of the user function

(*Wallace teaches the method includes the steps of generating fanout-free regions into quasi-canonical models("LUT"; col.8, lines 15-19) and transforming the result into swap structures so the pin swap groups and swappable pins can be identified (Fig.4;col. 5, lines 29-37); the swappable pins can be swapped or rotated as needed for modifying the circuit layout or configuration ("lookup table configurations")(Fig. 6-8; col. 9, lines 64+ to col. 13, line 26) if the designed specifications are not met (col. 1, lines 39-47; col. 7, lines 58-61; col. 14, lines 45-56). Wallace also teaches that the approach can be applied for mapping a design circuit into the LUT- based FPGAs as well (col. 8, lines 8-19; col. 14, lines 11-16).*

Referring to claim 2, Wallace discloses the method according to claim 1 further comprising:

decomposing the user function into a second set of decomposed functions *(Fig.4;col. 5, lines 29-37; Fig. 8; col. 13, lines 21-26*); and

determining whether the second set of decomposed functions can be implemented by one of the set of lookup table configurations for the programmable integrated circuit (*Fig.4;col. 5, lines 29-37*; *col. 1 , lines 39-47 and 61-65*).

Referring to claim 3, Wallace discloses the method according to claim 1 further comprising:

if the user function is not successfully decomposed into a set of decomposed

functions, rotating at least two of the input variables of the user function (*Wallace teaches that the method according to claim 1 further comprising the step of swapping pins if the circuit layout or configuration need to be modified; col. 1, lines 39-47*); and

attempting to decompose the user function into a second set of decomposed functions (*Fig. 4; col. 5, lines 29-37; col. 1 , lines 39-47 and 61-65*).

Referring to claim 8, Wallace discloses the method according to claim 1 wherein decomposing the user function into the first set of decomposed functions further comprises decomposing the user function into first stage functions and a second stage function, outputs of the first stage functions being inputs into the second stage function (*Fig. 6-8; col. 13, lines 21-26*).

Referring to claim 9, Wallace discloses the method according to claim 8 wherein rotating at least two of the input variables of the user function further comprises swapping at least one of the input variables of the first stage functions with at least one of the input variables of the second stage function (*Fig. 2, and 7-8; col. 3, lines 19-30*).

Referring to claim 10, Wallace discloses the method according to claim 9 further comprising:

attempting to decompose the user function into a second set of decomposed functions based on the rotated-input variables (*Fig. 7-8; col. 12, lines 26+; col. 13, lines 1-26*).

Referring to claim 11, Wallace discloses the computer program product stored on a computer readable medium for mapping a user function for a programmable integrated circuit to lookup tables *(col. 9, lines 15-20; col. 15, lines 36-49)*, the computer program product comprising:

code for decomposing the user function into a first set of decomposed functions, wherein the user function receives input variables (*Wallace teaches the step of decomposition a design circuit ("user function") into one or more fanout-free regions ("decomposed functions"); col. 1, lines 40-45, lines 61- 65; col. 2, lines 1-6; col. 4, lines 53+; col. 5, lines 1-28; col. 8, lines 13-19; col. 9, lines 15-20; col. 15, lines 36-49)*, the user function receiving input variables (*Fig. 1; col. 2, lines 15-16*);

code for determining whether the first set of decomposed functions can be performed by a configuration of lookup tables on the programmable integrated circuits, and

code for rotating at least two of the input variables of the user function if none of the configurations of lookup tables can implement the first set of decomposed functions (*Wallace teaches the method includes the steps of generating fanout-free regions into quasi-canonical models("LUT"; col.8, lines 15-19) and transforming the result into swap structures so the pin swap groups and swappable pins can be identified (Fig.4;col. 5, lines 29-37); the swappable pins can be swapped or rotated as needed for modifying the circuit layout or configuration ("lookup table configurations")(Fig. 6-8; col. 9, lines 64+ to col. 13, line 26) if the designed specifications are not met (col. 1, lines 39-47; col. 7, lines 58-61; col. 14, lines 45-56). Wallace also teaches that the approach can be applied for mapping a design circuit into the LUT- based FPGAs as well (col. 8, lines 8-19; col. 14, lines 11-16).*

Referring to claim 12, Wallace discloses the computer program product according to claim 11 further comprising;

code for rotating at least two of the input variables of the user function if the

user function is not successfully decomposed into a set of decomposed functions *(col. 1, lines 39-47; col. 15, lines 36-49)*; and

code for attempting to decompose the user function into a second set of decomposed functions (*col. 15, lines 36-49*).

Referring to claim 13, Wallace discloses the computer program product according to claim 11 wherein the code for decomposing the user function into the first set of decomposed functions further comprises code for decomposing the user function into first stage functions and a second stage function, outputs of the first stage functions being inputs into the second stage function (*Fig. 6-8; col. 13, lines 21-26; col. 15, lines 36-49*).

Referring to claim 14, Wallace discloses the computer program product according to claim 13 wherein the code (*col. 15, lines 36-49*) for decomposing further comprises:

code for decomposing the user function into a second set of decomposed functions based on the rotated input variables (*col. 15, lines 36-49*), the second set of decomposed functions including first stage functions and a second stage function (*Fig. 6-8; col. 13, lines 21-26*), wherein at least two input variables of the first and the second stages of the a set of decomposed functions have been rotated with respect to input variables of the first and the second stages of the first set of decomposed functions (Fig. 7-8; *col. 15, lines 36-49*).

Referring to claim 16, Wallace discloses the computer program product according to claim 11 wherein the code for decomposing the first function into the second functions further comprises code for decomposing the first function into the second functions using a disjoint decomposition technique (*col. 15, lines 36-49; col. 4, lines 53+; col. 5, lines 1-28*).

Referring to claim 20, Wallace discloses the computer program product according to claim 11 further comprising:

code for decomposing the user function into a second set of decomposed functions based on the rotated input variables, if none of the configurations of lookup tables can implement the first set of decomposed functions (*col. 15, lines 36-49)*; and

code for determining whether the second set of decomposed functions can be implemented by one of the configurations of lookup tables for the programmable integrated circuit (*col. 15, lines 36-49*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 4-7, 15, and 17- 19 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Wallace (US Patent No. 6360352).

Referring to claim 4 and similarly recited claim17, Wallace substantially discloses all the elements in the claim 4 and claim 11, except the steps of:

(claim 4)

if one of the lookup table configurations can implement the first set of decomposed functions, placing lookup tables in the lookup table configuration into logic blocks on the programmable integrated circuit; and

configuring programmable routing resources to connect the logic blocks on the programmable integrated circuit.

(claim 17)

code for placing lookup tables in one of the lookup table configurations into logic blocks on the programmable integrated circuit, if that lookup table configurations can implement the decomposed functions; and

code for configuring programmable routing resources to connect the logic blocks on the programmable integrated circuit.

Wallace reference suggests that if LUTs of an FPGA do not have a pre-defined logic models, then a decomposion technique is performed to generate a decomposition functions to modify the FPGA logic function so the decomposition functions can be implemented into an arbitrary LUT by swapping or rotating some of input variables (input pins) (col. 14, lines 11-23).

Wallace reference suggests that a set of decomposition functions implemented into an arbitrary set of LUT configuration and the LUTs are arranged in the same block (Fig. 7-8). The reference also suggests that a FPGA resource routing is another step may need to be processed after the LUT mapping (col. 14, lines 11-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have such steps of if one of the lookup table configurations can implement the first set of decomposed functions, placing lookup tables in a lookup table configuration into logic blocks

and configuring programmable routing resources to connect the logic blocks on the programmable integrated circuits, because it would reduce unnecessary step of rotating the input variables to thereby saving time during mapping process.

Referring to claim 5 and similarly recited claims 7, 18, and 19 Wallace substantially discloses all the elements in the claim 4 and claim 11, except

(claims 5 and 18)

(the computer program product)wherein one of the lookup table configurations includes two 5-input lookup tables and one 6-input lookup table; and

(claims 7 and 19)

(the computer program product)wherein one of the lookup table configurations includes two 4-input lookup tables and one 6-input lookup table.

Wallace reference suggests that in Fig. 7-8, each decomposition function block (AND, OR, MUX) in the block configurations may have two or more input variables (col. 5, lines 21-28).

It would have been obvious one of ordinary skill in the art at the time of the invention to design primitive gates to have two 5-input (or two 4-input) lookup tables and one 6-input lookup table because this reduce number of lookup tables and logic blocks implemented within the programmable IC as required by design specification.

Claims 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wallace** in view of **Cong et al. (Cong)** entitled Boolean Matching for LUT-Based Logic Blocks With Applications to Architecture Evaluation and Technology Mapping (IEEE Transactions on Computer-Aided Design of Circuits and Systems, 20(9); 1077-1090)

Referring to claim 6, Wallace substantially discloses all the elements in the claim 4 except wherein at least two of the input variables are shared between two of the lookup tables.

Cong discloses the mapping method wherein at least two of the input variables are shared between two of the lookup tables (*Fig. 4, 6.g*)

Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wallace into the teachings of Cong because the shared inputs would provide depth minimization for mapping FPGA to thereby minimizing number of stages to reduce delay in the programmable IC (Cong; p. 1089, see the conclusion).

Referring to claim 15, Wallace substantially discloses all the elements in the claim 11 except

wherein the code for decomposing the first function into the second functions further comprises code for decomposing the first function into the second functions using a non-disjoint decomposition technique.

Cong discloses the mapping method wherein decomposing a function using a non-disjoint decomposition technique (*p. 1081*).

Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Wallace into the teachings of Cong because the non-disjoint decomposition would provide depth minimization for mapping FPGA to thereby minimizing number of stages to reduce delay in the programmable IC (*Cong; p. 1089, see the conclusion*).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

VUTHE SIEK
PRIMARY EXAMINER